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EXAMINER	
DAY, HERNG DER	

ART UNIT	PAPER NUMBER
2128	17

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/347,409	AKIMOTO ET AL.	
	Examiner	Art Unit	
	Herng-der Day	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-6 and 8-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-6 and 8-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to Applicants' Amendment (paper # 16) to Office Action dated July 2, 2003 (paper # 14), mailed December 2, 2003.

1-1. Claims 2-4, 8-10, and 13 have been amended; claims 2-6 and 8-14 are pending.

1-2. Claims 2-6 and 8-14 have been examined and rejected.

Specification

2. Applicants have amended the specification in paper # 16. Therefore, the objection to the specification in section 3 of paper # 14 has been withdrawn.

3. The amendment filed April 1, 2003, is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material, which is not supported by the original disclosure, is as follows:

(1) Amended sentences at lines 2-4 of page 4 and lines 15-17 of page 6 in the original specification, as described in page 13 of paper # 10. Please refer to the corresponding rejections under 35 U.S.C. 112, first paragraph, as detailed in section **6** below.

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Objections

4. The Examiner has acknowledged that claims 4 and 10 have been amended. The objection to the claims in section 5 of paper # 14 has been withdrawn.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 3-6 and 9-12 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

In paper # 10, Applicants have amended pages 4 and 6 of the Specification from "a signal passing between said two logic blocks connected to each other **by** a computer" to "a signal passing between said two logic blocks connected to each other **in** a computer". This amendment introduces new matter because changing the preposition from "**by** the computer" to "**in** the computer" not only changes the scope but also has no support in the original specification.

7. Claims 2, 4, 8-10, and 13-14 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

7-1. The amended claim 2 recites the limitation "wherein, in the step (a), the plurality of values V_C comprises **only** a first V_C value of a transistor connected directly to an input pin of the logic block and a second V_C value of a transistor connected directly to an output pin of the logic block". However, the new added limitation "**only**" does not appear to have support in the specification.

7-2. The amended claim 4 recites the limitation "ratios of delay time **degradations**". However, the new added limitation "**degradations**" does not appear to have support in the specification.

7-3. The amended claim 8 recites the limitation "wherein in process (a) the plurality of V_C values comprises **exclusively** a V_C value of a transistor connected directly to an input pin of the logic block and another V_C value a transistor connected directly to an output pin of the logic block". However, the new added limitation "**exclusively**" does not appear to have support in the specification.

7-4. The amended claim 9 recites the limitation "based on transistor property values only for transistors inside the logic block connected directly to **one of** the input pin and the output pin of the logic blocks". However, the new added limitation "**one of**" does not appear to have support in the specification.

7-5. The amended claim 10 recites the limitation "ratios of delay time **degradations**". However, the new added limitation "**degradations**" does not appear to have support in the specification.

7-6. The previously added claim 13 recites the limitation "wherein in the first calculation means, the plurality of V_C values includes exclusively a V_C value of a transistor connected directly to an input pin of the logic block and a V_C value of a transistor connected directly to an output pin of the logic block". However, the new subject matter "includes exclusively" does not appear to have support in the specification. Claim 14 is rejected as being dependent on the rejected claim 13.

8. Claims 3-6 and 9-12 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

For example, as described in lines 2-4 of page 4 and in lines 15-17 of page 6, the block-to-block delay time $T_{connect\_aged}$ is delay time of a signal passing between said two logic blocks connected to each other by a computer. However, it is unclear for one skilled in the art why two logic blocks are not connected to each other by only wire(s) or conductor(s) but by a computer. Accordingly, without undue experimentation, it is unclear how one skilled in the art may make and/or use the invention by calculating the block-to-block aged signal delay time $T_{connect\_aged}$ of two logic blocks connected to each other by a computer because the calculation of the delay time introduced by the computer has not been disclosed in the specification.

9. Claims 4, 6, 10, and 12 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As described in page 19, a logic block comprising three stage inverters each of which has the same delay time. When the input changes from low level to high level, λ is shown by expression (31) and when the input changes from high level to low level, λ is shown by expression (32). Based on expression (32), the delay time for input changes from high level to low level will be zero.

Also note, as defined in page 11, λ_{in} (λ_{out}) is the ratio of the delay time occurred at the input (output) pin to the delay time between the input pin and the output pin. Based on the above definition of λ, without undue experimentation, it is unclear for one skilled in the art why the value of λ in expression (31) is not 1 / 2 because in the middle stage the input changes from high level to low level with zero delay time. Similarly, without undue experimentation, it is unclear for one skilled in the art about expressions (33) and (34) for four stage inverters.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 2-3, 5, 8-9, 11, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwanishi et al., U.S. Patent 6,047,247 issued April 4, 2000, and filed December 5, 1997, in view of Fang et al., U.S. Patent 6,278,964 issued August 21, 2001 and filed May 29, 1998.

11-1. Regarding claim 2, Iwanishi et al. disclose a method of calculating, by the use of a computer, a numerical value V_A representative of a circuit property of a logic level circuit, from a numerical value V_B, which shows a block property of a logic block included in the logic level circuit, the method comprising:

(a) calculating the value V_B (delays of the cells, delays of the cell-to-cell wirings, column 6, lines 39-40) from a plurality of numerical values V_C (circuit information of the LSI, column 6, line 37),

(b) calculating the value V_A from the value V_B, and outputting the value V_A as a value representative of a circuit property of said logic level circuit (delay calculation of an LSI, column 6, lines 35-36),

However, Iwanishi et al. do not expressly disclose: (1) each value V_C of the plurality of numerical values V_C representing a transistor property of a transistor included in the logic block; and (2) the plurality of values V_C comprises a first V_C value of a transistor connected directly to an input pin of the logic block and a second V_C value of a transistor connected directly to an output pin of the logic block. Nevertheless, Iwanishi et al. do suggest that the calculation of V_B based on circuit information (circuit information, column 6, lines 35-40).

Fang et al. disclose a detailed description of the IC cell data 102, which specifies characteristics and properties of the cells in the IC that are to be included in the simulation for hot-carrier effects (Fang, column 5, lines 38-45). IC cell data 102 includes the device model data to determine voltages and currents at each node within the cells. The device model data includes time-based mathematical models that typically include a set of device parameters and a set of complex equations which must be solved to simulate device performance (Fang, column 6, line 12 through column 7, line 39). In other words, Fang et al. disclose that the circuit information needed for simulating the hot-carrier effects includes a set of device (transistor) parameters (property of a transistor) for all devices including transistors connected directly to an input pin and transistors connected directly to an output pin.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Iwanishi et al. to incorporate the teachings of Fang et al. to obtain the invention as specified in claim 2 because Fang et al. disclose in detail the circuit information, which will be the input for simulating the hot-carrier effects, as suggested by Iwanishi et al.

11-2. Regarding claim 3, Iwanishi et al. disclose a method of calculating, by the use of a computer, a delay time of a signal passing through a logic level circuit which consists of a plurality of logic blocks from pin-to-pin delay time, which is delay time of a signal passing between an input pin and an output pin of a logic block, and block-to-block delay time, which is delay time of a signal passing between two logic blocks connected to each other, comprising:

(a) calculating the pin-to-pin delay time, and the block-to-block delay time without calculating in aging caused by hot carrier effect (delay calculation step, column 4, lines 53-63);

(b) calculating variations of signal delay times caused by aging (delay degradation amount calculation step, column 4, line 63 to column 5, line 9); and,

(c) modifying the pin-to-pin delay time and the block-to-block delay time calculated in step (a) by the variations calculated in step (b), and outputting said modified values for use as values representative of circuit properties of said logic level circuit (after-deterioration delay calculation step, column 5, lines 9-13).

However, Iwanishi et al. do not expressly disclose: (1) step (a) based on a value of a transistor property of a transistor included in the logic block; and (2) step (b) based on V_C values comprising exclusively a transistor property of a transistor connected directly to the input pin and a transistor property of a transistor connected directly to the output pin. Nevertheless, Iwanishi

et al. disclose, "in FIG. 10, U1, U2, U3 are instances given to the cells" (column 7, lines 52-53), i.e., examples of a cell comprising a single inverter only. Iwanishi et al. also suggest that the delay calculation is conducted based on circuit information (circuit information, column 6, lines 35-40).

Fang et al. disclose a detailed description of the IC cell data 102, which specifies characteristics and properties of the cells in the IC that are to be included in the simulation for hot-carrier effects (Fang, column 5, lines 38-45). IC cell data 102 includes the device model data to determine voltages and currents at each node within the cells. The device model data includes time-based mathematical models that typically include a set of device parameters and a set of complex equations which must be solved to simulate device performance (Fang, column 6, line 12 through column 7, line 39). In other words, Fang et al. disclose that the circuit information needed for simulating the hot-carrier effects includes a set of device (transistor) parameters (property of a transistor) for all devices including transistors connected to an input pin and transistors connected to an output pin. For the single inverter cell disclosed by Iwanishi et al., the circuit information needed for simulating the hot-carrier effects includes exclusively a set of inverter (transistor) parameters (property of a transistor), wherein, the inverter connected directly to the input pin and connected directly to the output pin.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Iwanishi et al. to incorporate the teachings of Fang et al. to obtain the invention as specified in claim 3 because Fang et al. disclose in detail the circuit information, which will be the input for simulating the hot-carrier effects, as suggested by Iwanishi et al.

11-3. Regarding claim 5, Iwanishi et al. further disclose a method of calculating, by the use of a computer, a delay time occurred to a signal passing through a logic level circuit that consists of a plurality of logic blocks, comprising:

(a) calculating delay times of all said logic blocks according to the method as in claim 3 (delay calculation step, delay degradation amount calculation step, and after-deterioration delay calculation step, column 4, line 53 to column 5, line 13; and analysis of section **11-2** above); and,

(b) calculating and outputting for use as a value representative of a circuit property of said logic level circuit the delay time of the logic level circuit from the result of step (a) (deterioration is estimated, column 5, lines 13-16).

11-4. Regarding claim 8, Iwanishi et al. disclose a computer-readable medium incorporating a program of instructions for calculating a numerical value V_A, which shows a property of a logic level circuit, from a numerical value V_B, which shows a property of a logic block constituting the logic level circuit, the program making a computer execute the following processes:

(a) calculating the V_B value (delays of the cells, delays of the cell-to-cell wirings, column 6, lines 39-40) from a plurality of numerical values V_C (circuit information of the LSI, column 6, line 37),

(b) calculating the V_A value from the V_B value, and outputting the V_A value for use as a value representative of a circuit property of said logic level circuit (delay calculation of an LSI, column 6, lines 35-36).

However, Iwanishi et al. do not expressly disclose: (1) each V_C value showing a property of a transistor constituting part of the logic block; and (2) the plurality of V_C values comprises a V_C value of a transistor connected directly to an input pin of the logic block and another V_C value

of a transistor connected directly to an output pin of the logic block. Nevertheless, Iwanishi et al. do suggest that the calculation of V_B based on circuit information (circuit information, column 6, lines 35-40).

Fang et al. disclose a detailed description of the IC cell data 102, which specifies characteristics and properties of the cells in the IC that are to be included in the simulation for hot-carrier effects (Fang, column 5, lines 38-45). IC cell data 102 includes the device model data to determine voltages and currents at each node within the cells. The device model data includes time-based mathematical models that typically include a set of device parameters and a set of complex equations which must be solved to simulate device performance (Fang, column 6, line 12 through column 7, line 39). In other words, Fang et al. disclose that the circuit information needed for simulating the hot-carrier effects includes a set of device (transistor) parameters (property of a transistor) for all devices including transistors connected directly to an input pin and transistors connected directly to an output pin.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Iwanishi et al. to incorporate the teachings of Fang et al. to obtain the invention as specified in claim 8 because Fang et al. disclose in detail the circuit information, which will be the input for simulating the hot-carrier effects, as suggested by Iwanishi et al.

11-5. Regarding claim 9, Iwanishi et al. disclose a computer-readable medium incorporating a program of instructions for calculating a delay time of a signal passing through a logic level circuit which includes a plurality of logic blocks from pin-to-pin delay time, which is delay time of a signal passing between an input pin and an output pin of a logic block, and block-to-block

delay time, which is delay time of a signal passing between two logic blocks connected to each other, the program configured to make a computer execute the following processes:

(a) calculating the pin-to-pin delay time and the block-to-block delay time without calculating in aging caused by hot carrier effect (delay calculation step, column 4, lines 53-63);

(b) calculating variations of signal delay times caused by aging (delay degradation amount calculation step, column 4, line 63 to column 5, line 9); and,

(c) modifying the pin-to-pin delay time and the block-to-block delay time calculated in step (a) by the variations calculated in step (b), and outputting said modified values for use as values representative of circuit properties of said logic level circuit (after-deterioration delay calculation step, column 5, lines 9-13).

However, Iwanishi et al. do not expressly disclose step (b) based on transistor property values only for transistors inside the logic block connected directly to the input pin and the output pin of the logic blocks. Nevertheless, Iwanishi et al. disclose, "in FIG. 10, U1, U2, U3 are instances given to the cells" (column 7, lines 52-53), i.e., examples of a cell comprising a single inverter only. Iwanishi et al. also suggest that the delay calculation is conducted based on circuit information (circuit information, column 6, lines 35-40).

Fang et al. disclose a detailed description of the IC cell data 102, which specifies characteristics and properties of the cells in the IC that are to be included in the simulation for hot-carrier effects (Fang, column 5, lines 38-45). IC cell data 102 includes the device model data to determine voltages and currents at each node within the cells. The device model data includes time-based mathematical models that typically include a set of device parameters and a set of complex equations which must be solved to simulate device performance (Fang, column 6, line

12 through column 7, line 39). In other words, Fang et al. disclose that the circuit information needed for simulating the hot-carrier effects includes a set of device (transistor) parameters (property of a transistor) for all devices including transistors connected to an input pin and transistors connected to an output pin. For the single inverter cell disclosed by Iwanishi et al., the circuit information needed for simulating the hot-carrier effects includes exclusively a set of inverter (transistor) parameters (property of a transistor), wherein, the inverter connected directly to the input pin and connected directly to the output pin.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Iwanishi et al. to incorporate the teachings of Fang et al. to obtain the invention as specified in claim 9 because Fang et al. disclose in detail the circuit information, which will be the input for simulating the hot-carrier effects, as suggested by Iwanishi et al.

11-6. Regarding claim 11, Iwanishi et al. further disclose a computer-readable medium incorporating a program of instructions for calculating a delay time occurred to a signal passing through a logic level circuit that consists of a plurality of logic blocks, the program making a computer execute the following processes:

(a) calculating delay times of all said logic blocks according to the program as in claim 9 (delay calculation step, delay degradation amount calculation step, and after-deterioration delay calculation step, column 4, line 53 to column 5, line 13; and analysis of section **11-5** above); and,

(b) calculating and outputting for use as a value representative of a circuit property of said logic level circuit the delay time of the logic level circuit from the result of step (a) (deterioration is estimated, column 5, lines 13-16).

11-7. Regarding claim 13, Iwanishi et al. disclose a signal delay calculation system which calculates the delay time of a signal passing through a logic level circuit consisting of a plurality of logic blocks, the system comprising:

first calculation means for calculating value V_B, a property of a logic block constituting the logic level circuit (delays of the cells, column 6, lines 39-40), based on a plurality of numerical values V_C (circuit information of the LSI, column 6, line 37),

second calculation means for calculating a value V_A, representing a signal delay property of a logic level circuit, from values V_B (delay calculation of an LSI, column 6, lines 35-36); and

output means for outputting value V_A (deterioration is estimated, column 5, lines 13-16).

However, Iwanishi et al. do not expressly disclose: (1) each V_C value representing a property of a transistor included in the logic block; and (2) the plurality of values V_C includes a V_C value of a transistor connected directly to an input pin of the logic block and a V_C value of a transistor connected directly to an output pin of the logic block. Nevertheless, Iwanishi et al. disclose, "in FIG. 10, U1, U2, U3 are instances given to the cells" (column 7, lines 52-53), i.e., examples of a cell comprising a single inverter only. Iwanishi et al. also suggest that the delay calculation is conducted based on circuit information (circuit information, column 6, lines 35-40).

Fang et al. disclose a detailed description of the IC cell data 102, which specifies characteristics and properties of the cells in the IC that are to be included in the simulation for hot-carrier effects (Fang, column 5, lines 38-45). IC cell data 102 includes the device model data to determine voltages and currents at each node within the cells. The device model data includes time-based mathematical models that typically include a set of device parameters and a set of

complex equations which must be solved to simulate device performance (Fang, column 6, line 12 through column 7, line 39). In other words, Fang et al. disclose that the circuit information needed for simulating the hot-carrier effects includes a set of device (transistor) parameters (property of a transistor) for all devices including transistors connected to an input pin and transistors connected to an output pin. For the single inverter cell disclosed by Iwanishi et al., the circuit information needed for simulating the hot-carrier effects includes exclusively a set of inverter (transistor) parameters (property of a transistor), wherein, the inverter connected directly to the input pin and connected directly to the output pin.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Iwanishi et al. to incorporate the teachings of Fang et al. to obtain the invention as specified in claim 13 because Fang et al. disclose in detail the circuit information, which will be the input for simulating the hot-carrier effects, as suggested by Iwanishi et al.

11-8. Regarding claim 14, Iwanishi et al. further disclose V_A is an aging delay property of a logic level circuit (deterioration in reliability of the LSI, column 5, lines 13-16).

Allowable Subject Matter

12. The equations of claims 4, 6, 10, and 12 are not expressly taught in the cited prior art of record, and would be allowable if the above rejections under 35 U.S.C. 112, first paragraphs are overcome.

Applicants' Arguments

13. Applicants argue the following:

13-1. (1) "Applicant respectfully submits that these amendments do not narrow the scope of the claims and do not raise any Festo implications" (page 13, first paragraph, paper # 16).

13-2. Rejection of Claims 3-6 and 9-12 under 35 U.S.C. §112

(2) "Applicant assumes that the Examiner intended to make a 'written description' rejection" (page 15, paper # 16).

(3) "the present invention deals with designing a semiconductor integrated circuit and in particular, with a method of verifying the reliability of the semiconductor integrated circuit" (page 15, paper # 16).

(4) "a person of ordinary skill would have understood that Applicant was in possession of the subject-matter concerning the connection of logic blocks of a semiconductor integrated circuit" (page 16, paper # 16).

(5) "the two logic blocks are connected to each other 'by a computer' meaning 'for,' or 'as part of,' 'a computer' application or environment" (page 16, paper # 16).

13-3. Rejection of Claims 13 and 14 under 35 U.S.C. §112

(6) "the Specification clearly states that hot-carrier effect for only the transistors connected to the input pin and the output pin is one possible way of providing the solutions disclosed" (page 17, paper # 16).

(7) "Equations (5) and (6) for the delay time of the pin-to-pin path make use only of the transistors connected to the input and output pins" (page 17, paper # 16).

13-4. Rejection of Claims 4, 6, 10, and 12 under 35 U.S.C. §112

(8) "For clarification purposes only, claims 4 and 10 have been amended to recite 'delay time degradations'" (page 18, paper # 16).

(9) "the relationship between the delay time and hot carrier damage is disclosed" (page 19, paper # 16).

13-5. Rejection of Claims 2-3, 5, 8-9, 11, 13, and 14 under 35 U.S.C. §103

(10) "neither Iwanishi nor Fang discloses or suggests a cell comprising only a single inverter. The Examiner has not cited any such disclosure or suggestion" (page 21, paper # 16).

(11) "Iwanishi and Fang do not disclose or suggest calculating a numerical value V_B from a plurality of values V_C comprising only ..., nor calculating variations of signal delay times, based on V_C values comprising exclusively ..." (page 21, paper # 16).

(12) "the Examiner does not explain why, without impermissible hindsight reconstruction, there would have been motivation to select from Fang any particular types of circuit information and combining them into Iwanishi to arrive at Applicant's invention" (page 22, paper # 16).

Response to Arguments

14. Applicants' arguments have been fully considered and they are not persuasive.

14-1. Response to Applicants' argument (1). Applicants' commentary is noted, but not agreed to. The claim amendments have changed the scope of the claims and thus raise Festo implications. Furthermore, Applicants' earlier amendments have already invoked Festo consideration.

14-2. Response to Applicants' argument (2). Applicants' commentary regarding 'written description' vs 'enablement' is noted. The Examiner makes a 'written description' rejection for "**in** the computer" amendment to the specification as detailed in section **6** above and an 'enablement' rejection for "**by** the computer" in the original specification as detailed in section **8** above. The rejections are clearly stated.

14-3. Response to Applicants' argument (3). Only the limitation of calculating "delay time" and "value representative of circuit property" has been claimed. A method of "verifying the reliability of the semiconductor integrated circuit" has not been claimed.

14-4. Response to Applicants' arguments (4) and (5). The Examiner respectfully disagrees with the Applicants' opinion. Although the language "by a computer" may make the claimed invention patentably distinguishing them from the references, it is unclear for one skilled in the art why two logic blocks are not connected to each other by only wire(s) or conductor(s) but by a computer. Accordingly, without undue experimentation, it is unclear how one skilled in the art may make and/or use the invention by calculating the block-to-block aged signal delay time $T_{connect\_aged}$ of two logic blocks connected to each other by a computer because the calculation of the delay time introduced by the computer has not been disclosed in the specification.

14-5. Response to Applicants' arguments (6) and (7). Applicants' arguments are directed to the calculating delay time due to hot-carrier effect. However, the Examiner's rejection is based on the conventional method for calculating delay time without reference to the hot electron effect.

For example, Even in Equation (6), T_{iopath_fresh}, which is the pin-to-pin delay time calculated ignoring aging caused by hot carrier effect as described at page 5 of the original specification, and the whole delay time occurred from the input pin to the output pin for

calculating λ cannot be calculated by "the plurality of values V_C includes **exclusively** a V_C value of a transistor connected directly to an input pin of the logic block and a V_C value of a transistor connected directly to an output pin of the logic block" as recited, for example, in claim 13.

Also notes, as described from the last line of page 12 to line 4 of page 13 in the original specification, "the delay time calculation 402 is a conventional method for calculating delay time without reference to the hot electron effect". Therefore, the Examiner respectfully submits that the limitation "includes exclusively", as recited in claim 13, for example, has no support in the original specification.

14-6. Response to Applicants' arguments (8) and (9). The Examiner respectfully disagrees with the Applicants' opinion. Based on the definition of λ as described in page 11 of the specification, adding "degradations" to claims 4 and 10 has no support in the original specification. The definition of λ seems inconsistent with expression (31) to (34). If supporting evidence exists, all the inconsistency should be corrected.

14-7. Response to Applicants' argument (10). Iwanishi et al. disclose, "in FIG. 10, U1, U2, U3 are instances given to the cells" (column 7, lines 52-53), i.e., examples of a cell comprising a single inverter only.

14-8. Response to Applicants' argument (11). The Examiner respectfully disagrees with the Applicants' opinion because the added limitation, for example, "exclusively" has no support in the original specification as detailed in section **14-5** above.

14-9. In response to Applicants' argument (12) that the Examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so

long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the Applicants' disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Conclusion

15. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Herng-der Day whose telephone number is (703) 305-5269. The examiner can normally be reached on 9:00 - 17:30.

If attempts to reach the examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin J Teska can be reached on (703) 305-9704. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Herng-der Day
February 17, 2004

HUGH JONES, Ph.D.
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